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09/927,675	08/10/2001	Guy Perry	MTI-31471	6524

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/927,675	PERRY, GUY	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 2, 4 - 23, 26 - 28, 30 - 34, 50 - 55, 57 - 65 and 69 - 78* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 2, 4 - 23, 26 - 28, 30 - 34, 50 - 55, 57 - 65 and 69 - 78* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 14, 2004 has been entered. An action on the RCE follows.

Response to Amendment

2. Applicant's amendment filed on November 16, 2004 has been received and entered in the case.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 28, 30 – 34, 74 and 76 rejected under 35 U.S.C. 102(b) as being anticipated by Preslar et al. (U.S. Pat. No. 5,900,643).

Regarding claim 28, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 a bond pad structure (36) in a semiconductor die (6a), comprising:

- a first bond pad (42 and 42a) and a second bond pad (40 and 40a);
- each of the bond pads comprising at least a lower metal layer and an upper metal layer;
- with a lower metal layer (40a) of one of the bond pads (40 and 40a) extending beneath the upper metal layer (42) of the other bond pads (42 and 42a); and
- at least one of the bond pads (40) functions to supply data, test a device, or supply various voltage levels (claim 28);
- wherein the first bond pad (42 and 42a) is functional only in an operational mode, and the second bond is functional in a test mode and in an operational mode (column 5, lines 28 – 32. Pad 40 is used for testing (e.g., probe 50) and operation (e.g., bond pad 52) while pad 42 is used only for operation (e.g., bond pad 52)). Furthermore, Preslar et al. discloses the lower metal layer (40a) of the second bond pad (40 and 40a) extending beneath or underneath the upper metal layer (42) of the first bond pad (42 and 42a; claim 31).

Alternatively, the limitation "wherein the first bond pad is functional only in an operational mode" is intended use or functional language which does not differentiate the claimed structure over Preslar et al. As such, pad 40 and 40a may be considered the "first" pad comprising a lower layer that extends beneath the upper layer 42 of the second pad and thus anticipate claims 30 and 32 – 34, because terms such as "first" and "second" are merely relative terms, which do not patternably distinguish claimed structure over Preslar et al.

Regarding claim 74, Preslar et al. discloses in e.g., Fig. 3, Fig. 4, column 5, lines 28 – 32 and column 6, lines 18 – 52 an integrated circuit supported by a substrate and comprising a bond pad structure (36), the bond pad structure comprising:

- a lower metal layer (40a and 42a) comprising first (40a) and second (42a) portions with a space (66a) therebetween;
- a dielectric layer (the layer in 66 and 66a) overlying the lower metal layer and within the space;
- at least one opening extending through the dielectric layer to each of the first and second lower metal portions; and
- an upper metal layer (40 and 42) overlying the dielectric layer and within the openings in the dielectric layer in contact with the first and second portions of the lower metal layer;
- the upper metal layer (40 and 42) comprising first (40) and second (42) portions, the first upper metal portion (40) positioned over the first lower metal portion (40a) to form a first bond pad, and the second upper metal portion (42) positioned over the second lower metal portion (42a) to form a second bond pad; and
- the upper metal portion (42) of one (42 and 42a) of the bond pads extends over the lower metal portion (40a) of the other bond pad (40 and 40a);
- wherein the first bond pad (42 and 42a) is functional solely in an operational mode, and the second bond is functional in a test mode and in an operational mode upon discontinuing the test mode and being interconnected to the first bond pad (column 5,

lines 28 – 32. Pad 40 is used for testing (e.g., probe 50) and operation (e.g., bond pad 52) while pad 42 is used solely for operation (e.g., bond pad 52)).

Furthermore, the limitation "wherein the first bond pad is functional solely in an operational mode" is intended use or functional language which does not differentiate the claimed structure over Preslar et al.

Regarding claim 76, Preslar et al. discloses in e.g., Fig. 3, Fig. 4, column 5, lines 28 – 32 and column 6, lines 18 – 52 a semiconductor wafer, comprising:

- a substrate (72) and a bond pad structure (36) disposed on the substrate, the bond pad structure comprising a first bond pad (40 and 40a) and a second bond pad (42 and 42a);
- each of the bond pads comprising a lower metal layer and an overlying upper metal layer; and
- the upper metal layer (42) of one (42 and 42a) of the bond pads extends beyond the lower metal layer (42a) of the one bond pad and over the lower metal layer (40a) of the other (40 and 40a) of the bond pads;
- wherein the first bond pad (40 and 40a) is functional only in an operational mode, and the second bond is functional in a test mode and in an operational mode (column 5, lines 28 – 32. Pad 40 is used for testing (e.g., probe 50) and operation (e.g., bond pad 52) while pad 42 is used only for operation (e.g., bond pad 52)).

Furthermore, the limitation "wherein the first bond pad is functional only in an operational mode" is intended use or functional language which does not differentiate the claimed apparatus over Preslar et al.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 4 – 23, 26, 27, 50 – 55, 57 – 65, 69, 70 – 73, 75, 77 and 78 are rejected under 35 U.S.C. 103(a) as being unpatentable over Preslar et al. (U.S. Pat. No. 5,900,643) in view of Ellis-Monaghan et al. (U.S. Pat. No. 6,495,917).

Regarding claims 1, 2, 9, 17 and 70, Preslar et al. discloses in e.g., Fig. 3 and Fig. 4 a bond pad structure (36) disposed on a substrate (72; claim 70) in a semiconductor die (6a; column 4, line 54), comprising:

- a bond pad structure (36) disposed on a substrate (72; claim 70);
- a first bond pad (40 and 40a) and second bond pad (42 and 42a);
- each of the bond pads comprising a lower metal layer and an upper metal layer;
- with the lower metal layer (40a) of one (40 and 40a) of the bond pads extending underneath the upper metal layer (42) of the other (42 and 42a) of the bond pads;
- wherein the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric layer (dielectric material) between the first and second bond pads to a substrate underlying the bond pads (claims 2, 9 and 17; see Fig. 4 and column 6, lines 18 - 52).

However, Preslar et al. does not disclose the pad having a plurality of lower metal layers. Ellis-Monaghan et al. teaches in e.g., Fig. 36 and column 7, line 51 – column 8, line 23 a pad (LM-1 – LM-3 and 361) having a plurality of lower metal layers (LM-1 – LM-3) under an upper metal layer (361). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Preslar et al. by adding another lower metal layer on the lower metal layer of Preslar et al. as taught by Ellis-Monaghan et al. The ordinary artisan would have been motivated to modify Preslar et al. in the manner described above for at least the purpose of adding support to the inter-layer dielectric (ILD) during wire or C4 bonding processes (column 4, lines 17 – 22).

Regarding claim 4, Preslar et al. and Ellis-Monaghan et al. disclose at least two lower metal layers of the one of the bond pads extend underneath the upper metal layer of the other of the bond pads.

Regarding claim 5, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 - 32 further comprising a conductive material (52, at the joint portion of the wire) interconnecting the first bond pad to the second bond pad.

Claims 6, 15, 20 and 54, Preslar et al. does not disclose the conductive material comprising a solder material or solder. However, Ellis-Monaghan et al. teaches in e.g. Fig. 34 a conductive material (345) comprising a solder material or solder (column 7, line 61). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Preslar et al. by using the solder material or solder for the conductive material as taught by Ellis-Monaghan et al. The ordinary artisan would have been motivated to modify

Preslar et al. in the manner described above for at least the purpose of increasing the bond strength between the pads and the external device (e.g., wire; column 8, lines 26 – 27).

Regarding claim 7, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 - 32 the conductive material (52, at the joint portion of the wire) overlies at least a portion of each of the first and second bond pads.

Regarding claim 8, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 - 32 further comprising a bonding wire (the terminal wire) connected to the conductive material.

Regarding claim 10, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 - 32 further comprising a conductive material (52, at the joint portion of the wire) interconnecting and overlying at least a portion of the first and second bond pads.

Regarding claims 11, 13, 18, 50, 51, 58 – 60 and 69, Preslar et al. discloses in e.g., Fig. 3 and Fig. 4 a bond pad structure (36) in a semiconductor die (6a), comprising:

- a first bond pad (40 and 40a) and a second bond pad (42 and 42a) positioned within a single passivation opening (under 36; claims 18, 50, 58 and 60);
- a first (40 and 40a) and second bond pad (42 and 42a) internonnected by a conductive material (52, at the joint portion of the wire; claim 13) overlying at least a portion of each of the bond pads (see Fig. 3; claims 18, 59 and 60);
- each of the bond pads comprising at least a lower metal layer and an upper metal layer; and
- with the lower metal layer (40a) of the first bond pad (40 and 40a) extending beneath the upper metal layer (42) of the second bond pad (42 and 42a; claim 51);

- wherein the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric layer (dielectric material) between the first and second bond pads to a substrate underlying the bond pads (claim 58; see Fig. 4 and column 6, lines 18 - 52).

However, Preslar et al. does not disclose the each (e.g., claim 69) bond pad comprising at least two lower metal layers. Ellis-Monaghan et al. teaches in e.g., Fig. 36 and column 7, line 51 – column 8, line 23 a pad (LM-1 – LM-3 and 361) having a plurality of lower metal layers (LM-1 – LM-3) under an upper metal layer (361). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Preslar et al. by adding another lower metal layer on the lower metal layer of Preslar et al. as taught by Ellis-Monaghan et al. The ordinary artisan would have been motivated to modify Preslar et al. in the manner described above for at least the purpose of adding support to the inter-layer dielectric (ILD) during wire or C4 bonding processes (column 4, lines 17 – 22).

Regarding claim 12, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 a bond pad structure (36) in a semiconductor die (6a), comprising:

- a first bond pad (42 and 42a) and a second bond pad (40 and 40a);
- each of the bond pads comprising at least a lower metal layer and an upper metal layer;
- with a lower metal layer (40a) of the second bond pad (40 and 40a) extending beneath the upper metal layer (42) of the first bond pad (42 and 42a).

Further, terms such as "first" and "second" are merely relative terms, which do not patternably distinguish claimed structure over Preslar et al.

However, Preslar et al. does not disclose the pad having at least two lower metal layers. Ellis-Monaghan et al. teaches in e.g., Fig. 36 and column 7, line 51 – column 8, line 23 a pad (LM-1 – LM-3 and 361) having a plurality of lower metal layers (LM-1 – LM-3) under an upper metal layer (361). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Preslar et al. by adding another lower metal layer on the lower metal layer of Preslar et al. as taught by Ellis-Monaghan et al. The ordinary artisan would have been motivated to modify Preslar et al. in the manner described above for at least the purpose of adding support to the inter-layer dielectric (ILD) during wire or C4 bonding processes (column 4, lines 17 – 22).

Regarding claim 14, Preslar et al. discloses in e.g., Fig. 3 and Fig. 4 the conductive material overling a portion of each of the bond pads.

Regarding claims 16 and 21, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 further comprising a bonding wire (the terminal wire) connected to the conductive material.

Regarding claim 19, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 7, lines 22 – 26 a passivation layer (the passivation layer) overlying a portion of each of the bond pads, the opening (at the place of 36) being through the passivation layer to expose the bond pads.

Claims 22 and 71, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 a bond pad structure (36) in a semiconductor die (6a), comprising:

- a first metal layer (40a and 42a) deposited onto a substrate (72) and patterned to form first (40a) and second (42a) lower metal layer portions having a space thereinbetween;

- a dielectric layer (a material in 66 and 66a) deposited over the first and second lower metal layer portions and the substrate within the space (66a), and etched to form openings (66) to each of the first and second lower metal layer portions; and
- a second metal layer (40 and 42) deposited over the dielectric layer and into the openings of the dielectric layer and etched to form a first (40) and second (42) upper metal layer portions overlying and in conductive contact with the first and second lower metal layer portions;
- the first upper (40) and lower (40a) metal layer portions forming a first bond pad, and the second upper (42) and lower (42a) metal layer portions forming a second bond pad;
- a conductive material (52, at the joint portion of the wire) situating on and interconnecting the first bond pad and the second bond pad (see Fig. 3);
- wherein a lower metal layer (40a) portion of one (40 and 40a) of the bond pads extends beneath the upper metal layer (42) portion of the other (42 and 42a) of the bond pads
- the upper metal portion (42) of one (42 and 42a) of the bond pads extends over the lower metal portion (40a) of the other (40 and 40a) bond pad (claim 71).

However, Preslar et al. does not disclose the conductive material comprising a solder material or solder. However, Ellis-Monaghan et al. teaches in e.g. Fig. 34 a conductive material (345) comprising a solder material or solder (column 7, line 61). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Preslar et al. by using the solder material or solder for the conductive material as taught by Ellis-

Monaghan et al. The ordinary artisan would have been motivated to modify Preslar et al. in the manner described above for at least the purpose of increasing the bond strength between the pads and the external device (e.g., wire; column 8, lines 26 – 27).

Regarding claim 23, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 7, lines 22 – 26 a passivation layer (the passivation layer) formed over the bond pads and etched to form an opening (at the place of 36) therethrough to expose the first and second bond pads.

Regarding claim 26, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 the conductive material overlies at least a portion of each of the first and second bond pads.

Regarding claim 27, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 further comprising a bonding wire (the terminal wire) connected to the conductive material.

Regarding claims 52, 61 and 62, a further difference between Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 an integrated circuit die (6a), comprising:

- a first bond pad (42 and 42a) interconnected to a second bond pad (40 and 40a), the first and second bond pads being positioned within a single passivation (the passivation layer) opening (at the place of 36; claim 61);
- each of the first and second bond pads comprising at least a lower metal layer and an upper metal layer;
- with a lower metal layer (40a) of one (40 and 40a) of the bond pads extending underneath the upper metal layer (42) of the other (42 and 42a) of the bond pads;
- the lower metal layer (40a) of the second bond pad (40 and 40a) extending underneath the upper metal layer (42) of the first bond pad (42 and 42a); and

- at least one of the bond pads functional to supply data, retrieve data, test a device, or supply various voltages (claim 62).

Further, terms such as "first" and "second" are merely relative terms, which do not patternably distinguish claimed structure over Preslar et al.

However, Preslar et al. does not disclose the pad having at least two lower metal layers. Ellis-Monaghan et al. teaches in e.g., Fig. 36 and column 7, line 51 – column 8, line 23 a pad (LM-1 – LM-3 and 361) having a plurality of lower metal layers (LM-1 – LM-3) under an upper metal layer (361). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Preslar et al. by adding another lower metal layer on the lower metal layer of Preslar et al. as taught by Ellis-Monaghan et al. The ordinary artisan would have been motivated to modify Preslar et al. in the manner described above for at least the purpose of adding support to the inter-layer dielectric (ILD) during wire or C4 bonding processes (column 4, lines 17 – 22).

Regarding claim 53, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 a conductive material (52, at the joint portion of the wire) interconnecting and overlying at least a portion of the first bond pad and the second bond pad.

Regarding claim 55, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 a bonding wire (the terminal wire) connected to at least one of the bond pads.

Regarding claim 57, Preslar et al. discloses in e.g., Fig. 4, and column 6, lines 18 - 52 the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric material between the first and second bond pads to a substrate underlying the bond pads.

Regarding claims 63 and 65, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 a conductive material (52, at the joint portion of the wire) interconnecting and overlying at least a portion of each of the bond pads.

Regarding claim 64, Preslar et al. discloses in e.g., Fig. 3, Fig. 4, column 5, lines 28 – 32 and column 6, lines 18 – 52 the first bond pad (42 and 42a) being functional to receive and respond to a test mode signal by entering a test mode, and the second bond pad (40 and 40a) being functional in an operational mode, and upon discontinuing the test mode and being interconnected to the second bond pad, the first and second bond pads are functional to receive and respond to an operational mode signal by entering an operational mode.

Regarding claims 72 and 73, Preslar et al. discloses in e.g., Fig. 3, Fig. 4, column 5, lines 28 – 32 and column 6, lines 18 – 52 an integrated circuit supported by a substrate and comprising:

- a bond pad structure (36), the bond pad structure comprising two or more bond pads (40 & 40a and 42 & 42a; claim 72),
- a first bond pad (40 and 40a) and a second bond pad (42 and 42a);
- each of the bond pads comprising a lower metal layer and an overlying upper metal layer; and
- the upper metal layer (42) of one (42 and 42a) of the bond pads extends beyond the lower metal layer (42a) of the one bond pad and over the lower metal layer (40a) of the other (40 and 40a) of the bond pads.

However, Preslar et al. does not disclose the pad having at least two lower metal layers. Ellis-Monaghan et al. teaches in e.g., Fig. 36 and column 7, line 51 – column 8, line 23 a pad

(LM-1 – LM-3 and 361) having a plurality of lower metal layers (LM-1 – LM-3) under an upper metal layer (361). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Preslar et al. by adding another lower metal layer on the lower metal layer of Preslar et al. as taught by Ellis-Monaghan et al. The ordinary artisan would have been motivated to modify Preslar et al. in the manner described above for at least the purpose of adding support to the inter-layer dielectric (ILD) during wire or C4 bonding processes (column 4, lines 17 – 22).

Regarding claim 75, Preslar et al. discloses in e.g., Fig. 3, Fig. 4, column 5, lines 28 – 32 and column 6, lines 18 – 52 a semiconductor die (6a), comprising:

- a substrate (72); and
- a bond pad structure (36) disposed on the substrate (72), the bond pad structure comprising multiple bond pads (40 & 40a and 42 & 42a), each bond pad comprising overlying upper and lower metal layers, and the upper metal layer (42) of one of the bond pads (42 and 42a) overlaps the lower metal layer (40a) of another (40 and 40a) of the bond pads.

However, Preslar et al. does not disclose the pad having at least two lower metal layers. Ellis-Monaghan et al. teaches in e.g., Fig. 36 and column 7, line 51 – column 8, line 23 a pad (LM-1 – LM-3 and 361) having a plurality of lower metal layers (LM-1 – LM-3) under an upper metal layer (361). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Preslar et al. by adding another lower metal layer on the lower metal layer of Preslar et al. as taught by Ellis-Monaghan et al. The ordinary artisan would have been motivated to modify Preslar et al. in the manner described above for at least the

purpose of adding support to the inter-layer dielectric (ILD) during wire or C4 bonding processes (column 4, lines 17 – 22).

Claims 77 and 78, Regarding claim 75, Preslar et al. discloses in e.g., Fig. 3, Fig. 4, column 5, lines 28 – 32 and column 6, lines 18 – 52 a semiconductor wafer (6a), comprising:

- a semiconductor die (6a) comprising
    - o a substrate (72); and
    - o a bond pad structure (36) disposed on the substrate (72), the bond pad structure comprising a first bond pad (40 & 40a) and a second bond pad (42 & 42a) that are interconnected by a conductive material;
    - o each bond pad comprising an upper metal layer (42) overlying a lower metal layer, and the upper metal layer (42) of one of the bond pads (42 and 42a) overlapping at least one of the lower metal layer (40a) of another (40 and 40a) of the bond pads;
- wherein the first bond pad (40 and 40a) is functional solely in an operational mode, and the second bond is functional in a test mode and in an operational mode (column 5, lines 28 – 32; claim 78. Pad 40 is used for testing (e.g., probe 50) and operation (e.g., bond pad 52) while pad 42 is used solely for operation (e.g., bond pad 52)).

Furthermore, the limitation "wherein the first bond pad is functional solely in an operational mode" is intended use or functional language which does not differentiate the claimed structure over Preslar et al.

However, Preslar et al. does not disclose the pad having at least two lower metal layers and the conductive material comprising a solder material or solder. Ellis-Monaghan et al. teaches

in e.g., Fig. 34, Fig. 36 and column 7, line 51 – column 8, line 23 a pad (LM-1 – LM-3 and 361) having a plurality of lower metal layers (LM-1 – LM-3) under an upper metal layer (361) and a conductive material (345) comprising a solder material or solder (column 7, line 61). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Preslar et al. by adding another lower metal layer on the lower metal layer of Preslar et al. and using the solder material or solder for the conductive material as taught by Ellis-Monaghan et al. The ordinary artisan would have been motivated to modify Preslar et al. in the manner described above for at least the purpose of adding support to the inter-layer dielectric (ILD) during wire or C4 bonding processes (column 4, lines 17 – 22).

Response to Arguments

7. Applicant's arguments with respect to claims 1, 9, 11, 12, 13, 18, 22, 28, 32, 58, 60 – 62, 69 - 78 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
Thursday, February 03, 2005

GEORGE ECKERT
PRIMARY EXAMINER